Device reliability studies using low frequency noise measurements

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Outline

- Introduction to low frequency noise
- Devices under study
- Experimental setup
- Gate electric field stress experiment
- Channel electrical field stress experiment

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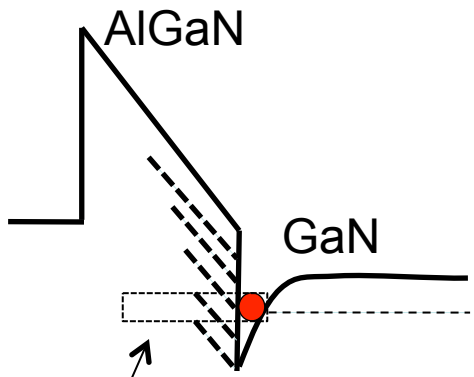
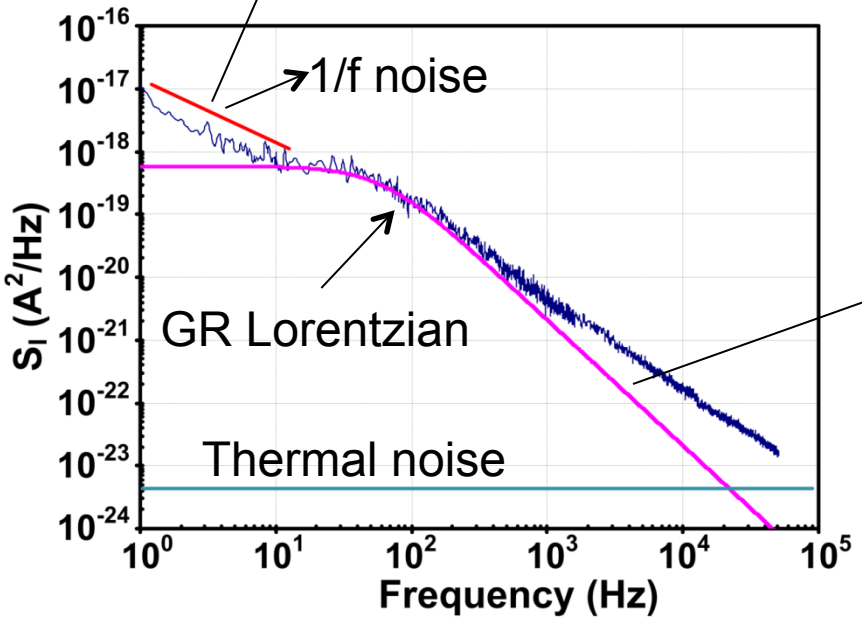
Defect spectroscopy using noise

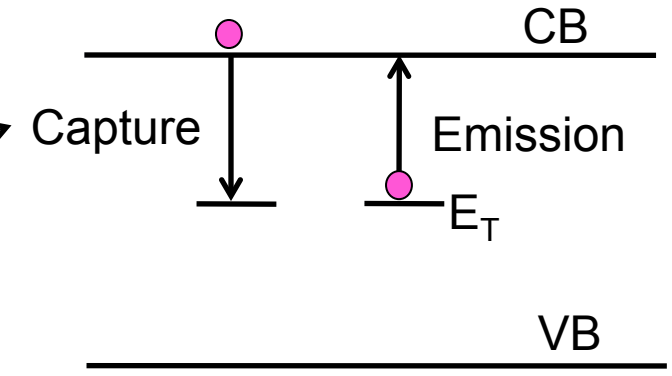


- $\frac{1}{f^{\gamma}}$ noise is an excellent *interface defect* quality indicator for the channel.

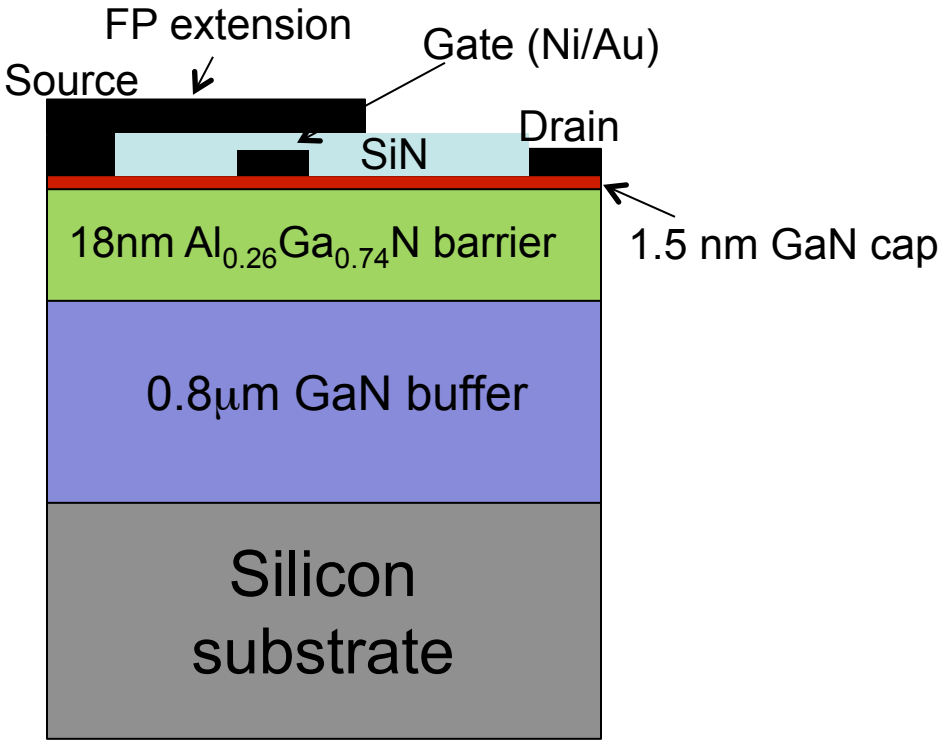
$$\frac{S_I}{I^2} = \frac{\alpha_H}{Nf}$$ where α_H is the Hooge parameter

- Lorentzian due to random telegraph noise is an excellent *point defect* probe.

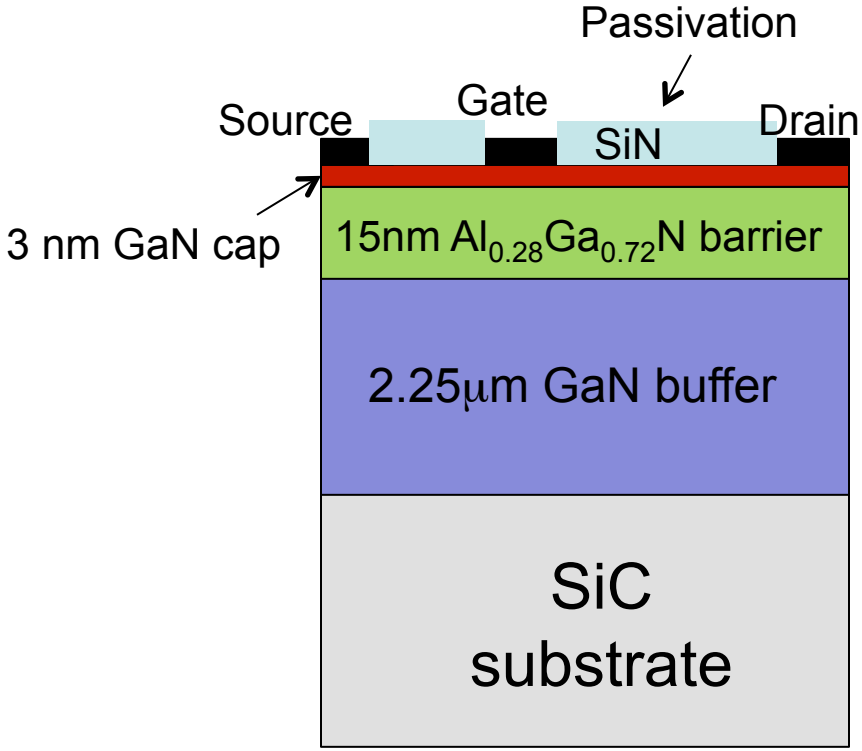




Devices under study

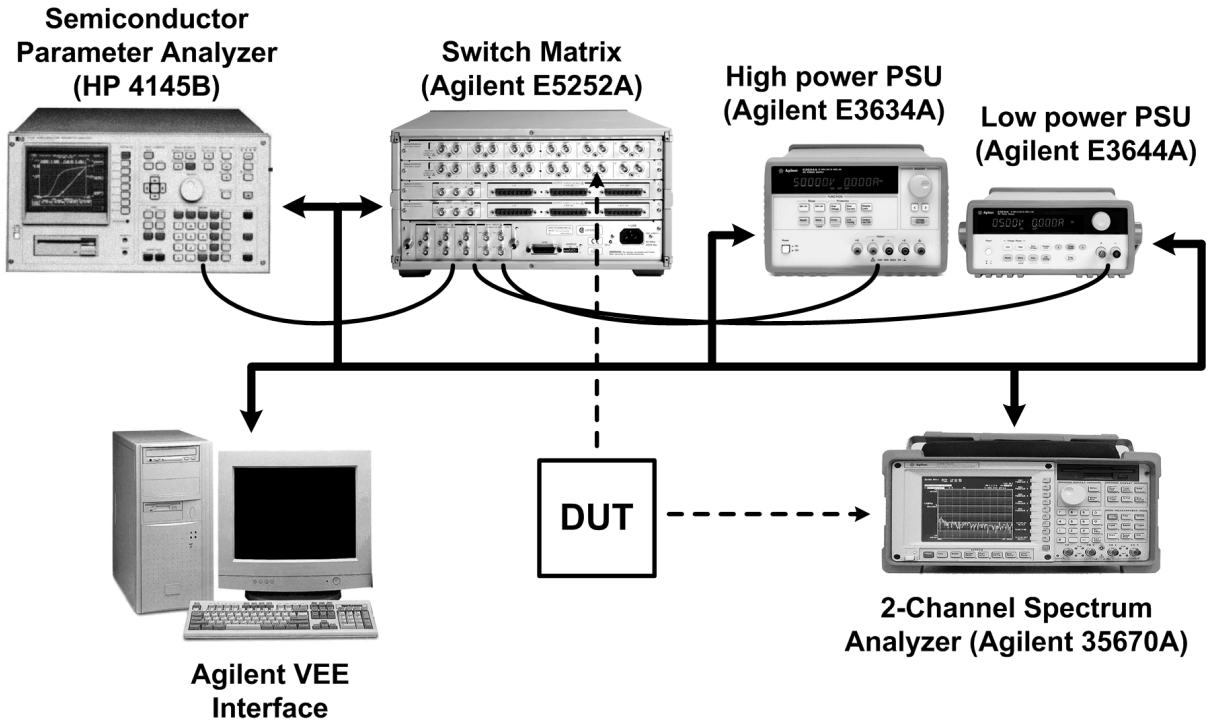


- Commercial device
- Gate length (L_G ~ 0.65 μm)
- 10 gate finger device with 2 mm periphery.
- Ceramic packaged.



- AFRL sample
- Gate length (L_G ~ 0.1 μm)
- 2 gate finger device with W_G ~ 160 μm
- Ceramic packaged.

Stress measurement setup



- Simultaneous high current (~ 4A) and voltage (~ 50 V) stress capability.
- Both SMU and PSU are programmable for step/stress/recovery type methodologies.
- Fully automated for both stress and noise measurements.

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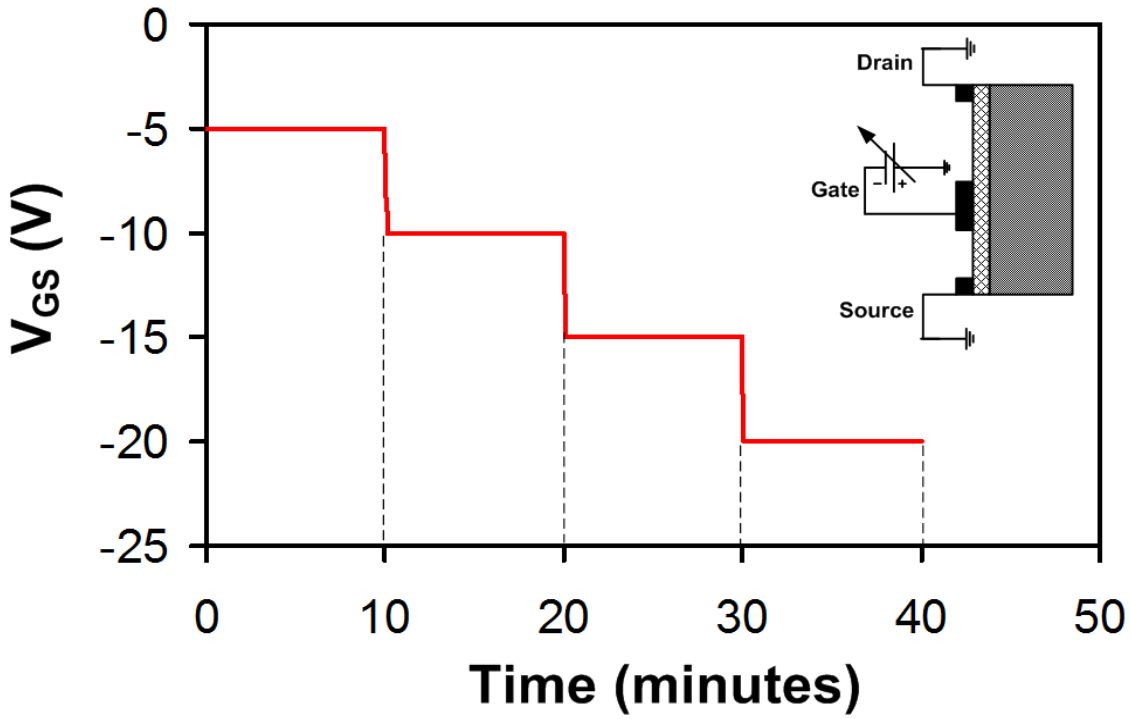
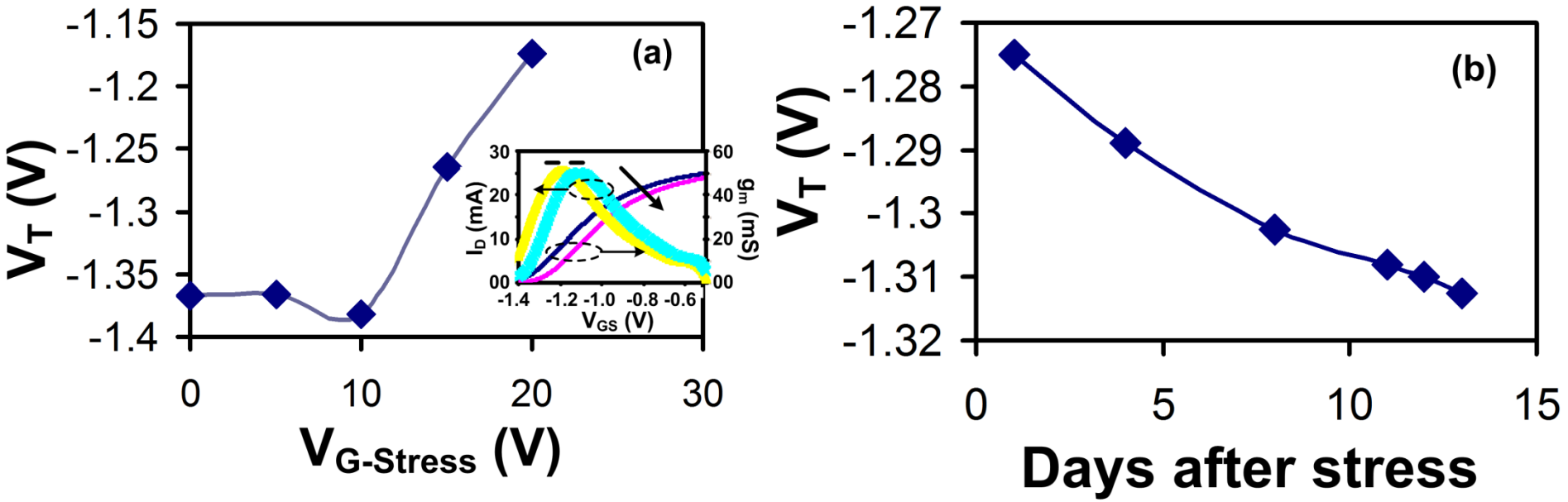
Gate stress experiment



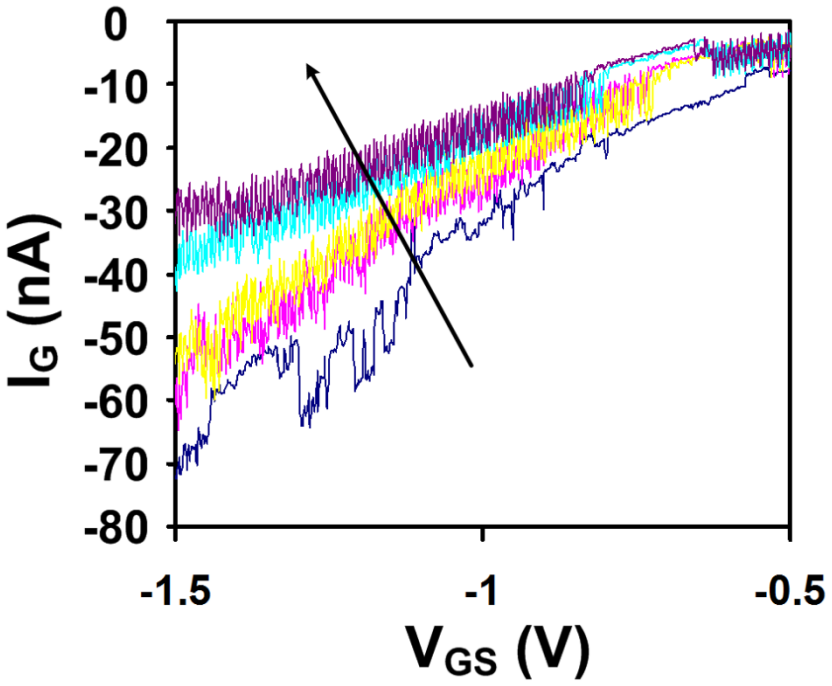
- Gate stack stressed from -5V to -20V for 10 minutes each with drain and source grounded.
- Transconductance I_G,I_D-V_G, Drain and Gate current noise measured between each stress bias.
- Device disconnected to the bias supplies after stress. Noise and I-V measurements were continued for several weeks thereafter.

DC transient effect



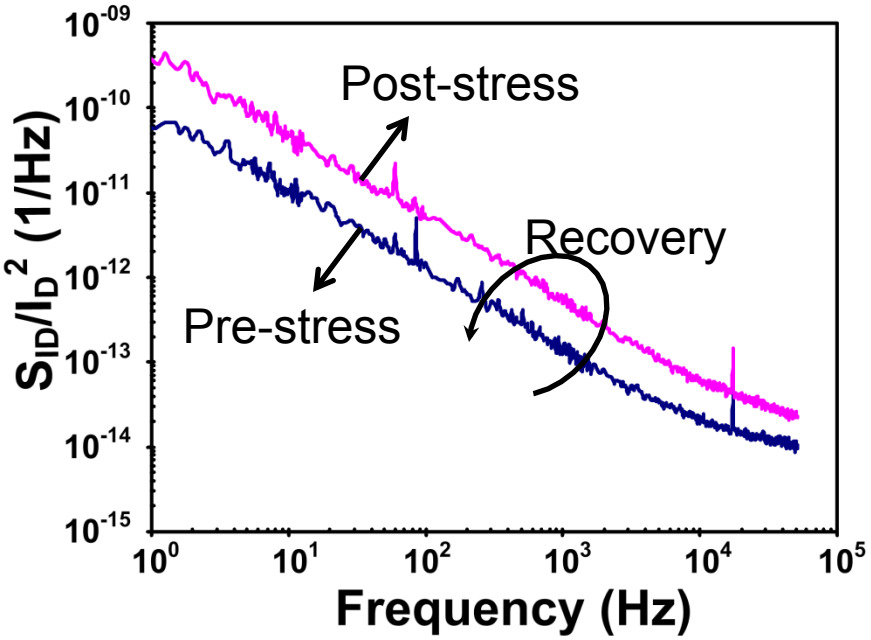
- Threshold voltage (V_T) constant till V_G = -10 V and then trends positive as V_G increases due to large trap filling under gate.
- V_T recovers to its pre-stress level subsequently by slowly becoming more negative. This is analogous to slow de-trapping of electrons beneath the gate. (Ref. Sahoo 2003)

DC transient effect



- Gate current during stress *decreases in magnitude* as a function of applied stress, can be explained by gate potential becoming more negative due to trap-filling under the gate stack during stress (Ref. Sahoo 2003).

Drain noise evolution



$$\because \frac{S_{I_D}}{I_D^2} \cong \frac{S_{R_{CH}}}{R_{CH}^2} = \frac{\alpha_{CH}}{N_{CH} f}$$

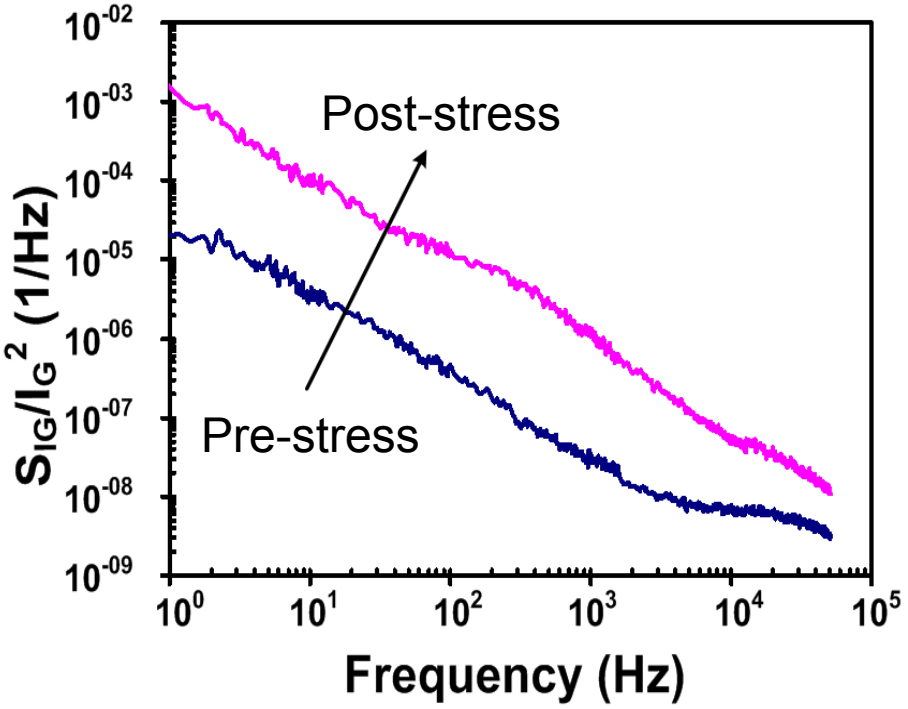
$$Where, N_{CH} = C_{AlGaN}(V_{GS} - V_T)$$

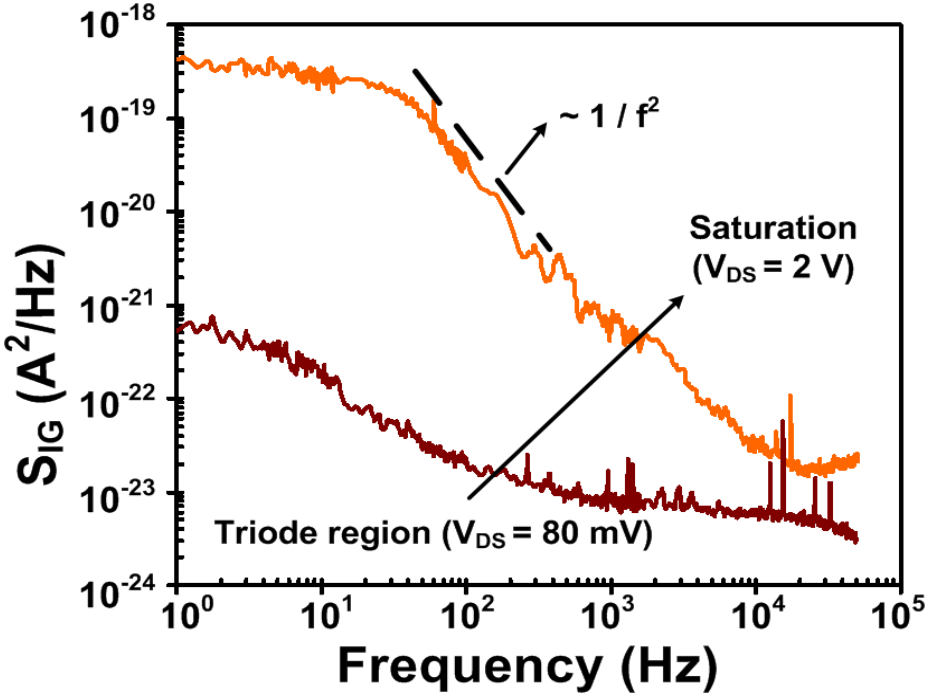
$\because V_{GS}$ is constant

$$\therefore V_T \downarrow \Rightarrow N_{CH} \uparrow \Rightarrow \frac{S_{I_D}}{I_D^2} \downarrow$$

- Drain current noise completely recovers to its pre-stress levels as threshold voltage becomes more negative due to de-trapping of electrons.
- *No channel degradation during or after the stress !!*

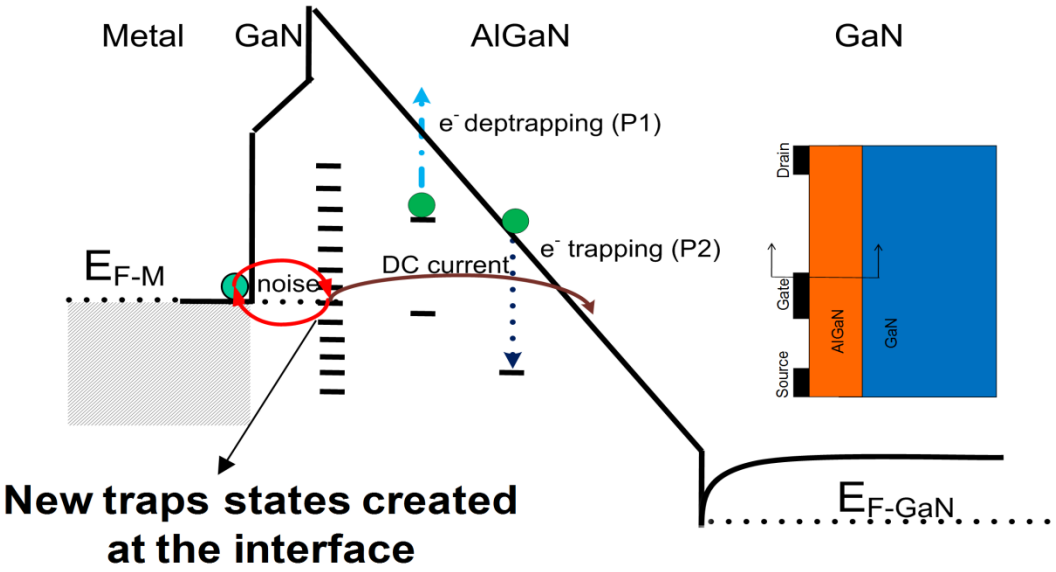
Gate noise evolution





- *Permanent degradation of the gate current noise !!*
- Increase of trap density located at the gate edges.

Degradation model



- Trap states are created at the GaN/AlGaN semiconductor interface during stress which leads to gate noise increase. Inverse piezo-electric effect is the possible explanation since not very high gate current densities (~0.038 A/mm^2) are involved during stress.
- Trap levels at the E_{F-M} quasi-Fermi level are likely candidates for modulating the trap assisted gate stack tunneling current.
- The DC transient effects are due to trap filling during stress and trap emptying after stress.

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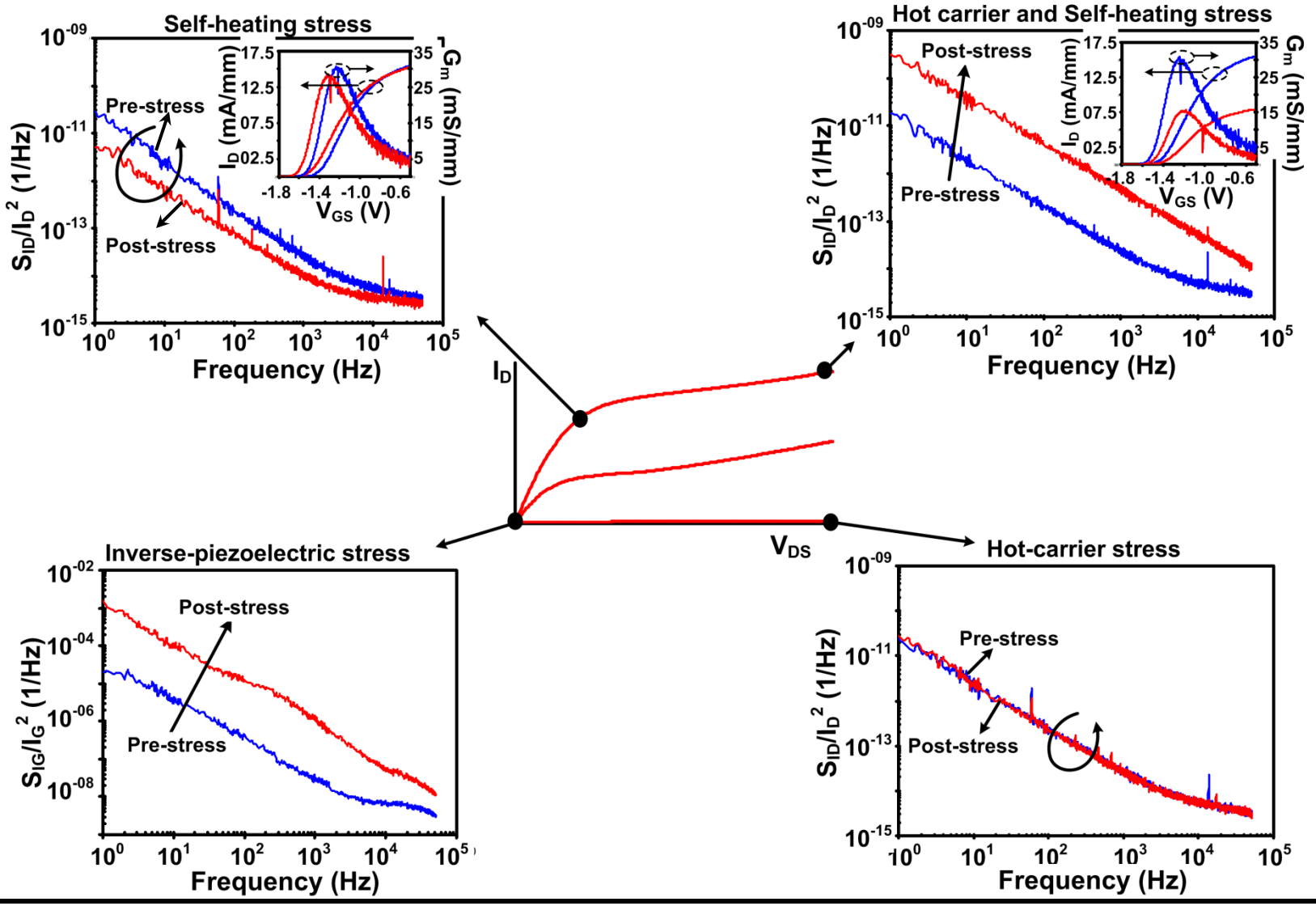
Channel stress experiment (GaN-on-Si)

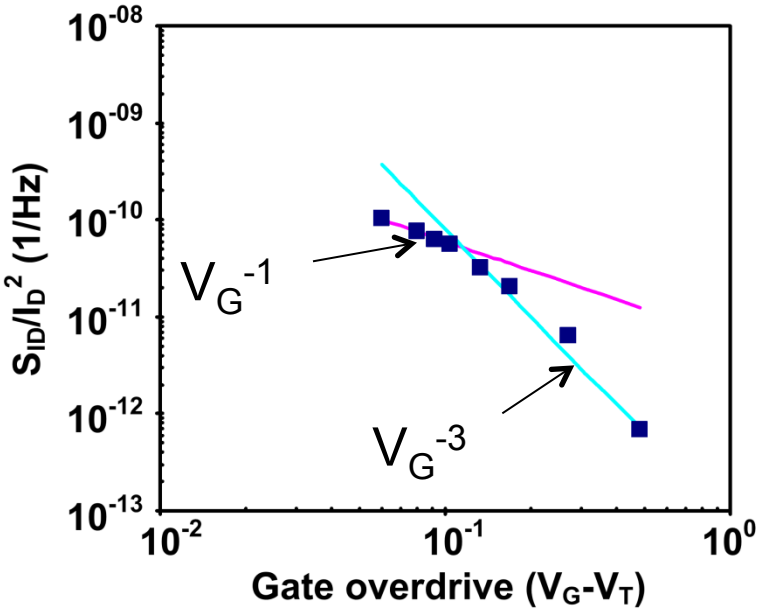
Test	V_{DS} (V)	V_{GS} (V)	P_{Dmax} (channel)	Stress time	Stress type
I	20	-1.7	2.3 W/mm	5 minutes	Hot carrier and self-heating
II	2	2	0.575 W/mm	30 minutes	Self-heating
III	10 to 30 step	-4	0.45 mW/mm	60 minutes	Hot-carrier

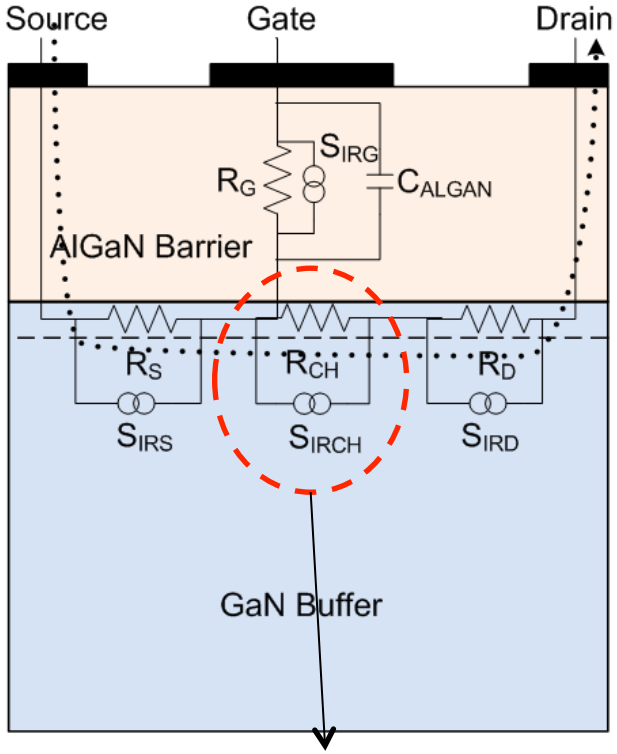
- Gate bias varied to control channel carriers and therefore, current.
- Transient and permanent changes observed in each stress condition.

Results


Self-heating stress
Pre-stress
Post-stress
S_{ID}/I_D^2 (1/Hz)
I_D (mA/mm)
G_m (mS/mm)
V_{GS} (V)
Frequency (Hz)
Hot carrier and Self-heating stress
Post-stress
Pre-stress
S_{ID}/I_D^2 (1/Hz)
I_D (mA/mm)
G_m (mS/mm)
V_{GS} (V)
Frequency (Hz)
I_D
V_{DS}
Inverse-piezoelectric stress
Post-stress
Pre-stress
S_{IG}/I_G^2 (1/Hz)
Frequency (Hz)
Hot-carrier stress
Pre-stress
Post-stress
S_{ID}/I_D^2 (1/Hz)
Frequency (Hz)

Analysis

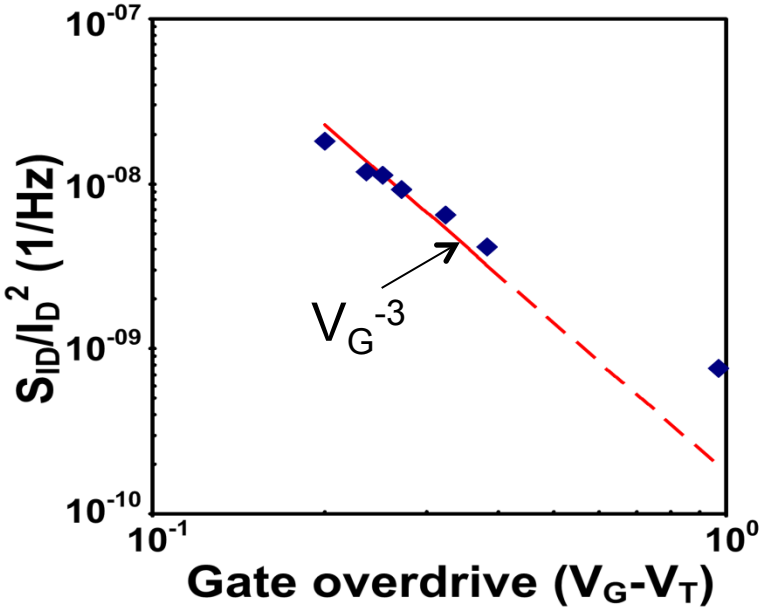


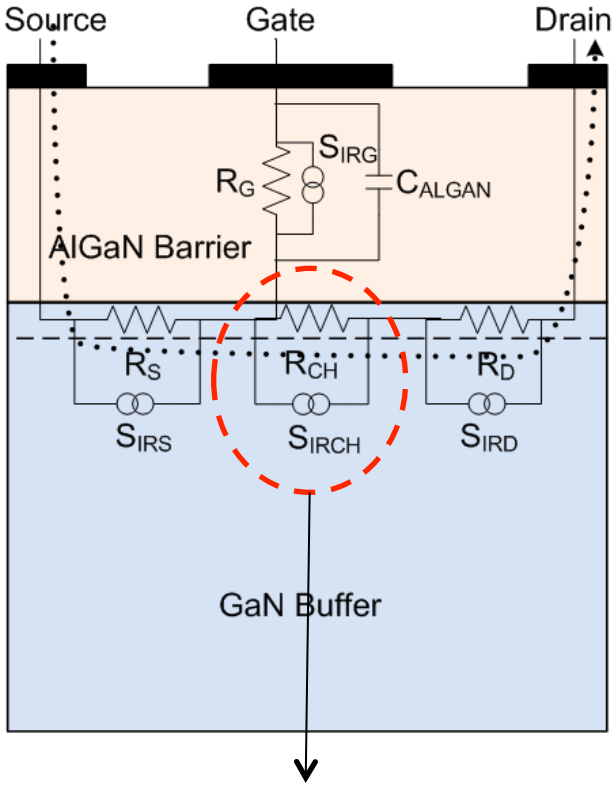


Degradation in the gated channel

- Increase of trap density at the AlGaN/GaN interface.
- Hooge parameter (α_H) changed from ~ 10^{-3} to 1.5×10^{-2}

Channel stress experiment (GaN-on-SiC)





Degradation in the gated channel

- Hot carrier and self-heating stress at constant V_{DS} = 25V, V_{GS}=0V, T=160s, and $P_{D\,max}$= 18.75W/mm
- Hooge parameter (α_H) changed from ~ 10^{-3} to 8.4×10^{-2}

Conclusions

- Characterized permanent trap creation and migration in the gate stack after high electric field stress.
- Characterized permanent degradation in the AlGaN/GaN interface after high electric field and self-heating stress.